REMARKS

Claims 1, 3, and 5-33 are pending in the application with the present amendments. Applicants reaffirm the election of Claims 1-12 which was provisionally made before this Official Action. Accordingly, claims 13-32 stand withdrawn from consideration. Claim 33 is added by way of the present amendment. The title has been amended herein to more clearly indicate the claimed invention.

In the Office Action, the Examiner rejected claims 1-6 and 8-11 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,703,648 to Xiang et al. ("Xiang"). Claims 1-7, 9 and 12 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Publication No. 2004/0065927 to Bhattacharyya ("Bhattacharyya"). For the reasons set forth below, Applicants respectfully submit that the presently pending claims overcome the rejections. Reconsideration and allowance of the claims are respectfully requested.

As amended herein, claim 1 now recites an integrated circuit having complementary metal oxide semiconductor (CMOS) transistors including a p-type field effect transistor (PFET) and an n-type field effect transistor (NFET). The PFET and the NFET each have a channel region and source and drain regions disposed in a first semiconductor region having a first composition. A first strain is applied to the channel region of the PFET but not to the channel region of the NFET via second semiconductor regions which have a second composition that is lattice-mismatched to the first semiconductor region. Claim 1 also recites that the second semiconductor regions underlie the source and drain regions of the PFET but do not underlie the channel region of the PFET and do not underlie the NFET.

Such structure is advantageous in that the second semiconductor regions underlying the source and drain regions of the PFET but not underlying the channel region produce a compressive strain in the channel region of the PFET but do not produce a compressive strain in the channel region of the NFET. In a particular example, as claimed in claims 6, 9 and 12, the channel regions and source and drain regions of the PFET and the NFET are disposed in regions consisting essentially of silicon and the second strain inducing semiconductor regions consist essentially of silicon germanium. As indicated in the specification at ¶[0031], advantageously, this arrangement produces a compressive strain in the PFET having a magnitude of between about 50 MPa and 2 GPa, and most preferably between about 200 MPa and 600 MPa.

By contrast, Bhattacharyya merely shows a structure in which a silicon germanium semiconductor region 26 is disposed underlying the entire strained semiconductor layer 40 in which the channel region and the source and drain regions of the transistor are disposed (FIG. 10, ¶¶[0075]-[0076], and ¶[0054]), and not merely underlying the source and drain regions of the PFET.

Similarly, in the transistor structure shown in Xiang (FIG. 3i), a silicon germanium layer 40 is disposed underlying the entire strained semiconductor layer including the source and drain extensions 68 and the strained silicon channel region 64 of the transistor. While Xiang describes the formation of silicon germanium regions 64 adjacent to ends of the channel regions (col. 5, lns. 30-65), Xiang also requires a silicon germanium layer 40 to underlie the entire strained semiconductor layer. In addition, Xiang teaches that the source and drain regions 72 and the source and drain extensions 68 are formed in the silicon germanium layer 40 and the silicon germanium regions 64. Xiang neither teaches nor suggests a transistor structure having source and

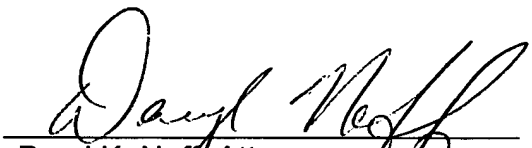
drain regions formed in a first semiconductor region having a first composition, e.g., silicon, and second semiconductor regions underlying the source and drain regions having a second composition, e.g., silicon germanium, to produce a strain in the channel region, in which the second semiconductor regions do not underlie the channel region of the transistor.

Support for the present amendments is provided, *inter alia*, at ¶[0022] and ¶[0038].

In view of the foregoing amendments and remarks, Applicants submit that the application is now in condition for immediate allowance. If for any reason the Examiner has any question regarding the content of this amendment or the allowability of the presently pending claims, he is respectfully requested to contact the Applicants' undersigned attorney at the telephone number indicated below.

It is believed that no fee is required upon filing this Amendment. However, if any fee is required, authorization is given to debit the Deposit Account No. 09-0458 of the Assignee for the amount due, and to credit any overpayment to the same account.

Respectfully submitted,
Huajie Chen et al.

By: 

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